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| EXAMINER | |
|---|---|
| INGHAM, JOHN C | |
| ART UNIT | PAPER NUMBER |
| 2814 | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/529,565 | FUERGUT ET AL. | |
| | Examiner | Art Unit | |
| | John C. Ingham | 2814 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *26 June 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *10-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 March 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

**DETAILED ACTION**

1. The Remarks filed 26 June 2007 have been entered. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims **10-25** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hoffman (US 6,737,750) and Ma (US 6,271,469).

4. Regarding claims **10 and 19-21**, Hoffman discloses in Fig 6A an electronic component comprising: a stack of semiconductor chips having a first semiconductor chip (12) and a stacked second semiconductor chip (16), the semiconductor chips having an active first face (12A, 16A) with contact pads (12C, 16C) to integrated circuits and a second face (12B, 16B); a flat conductor structure (14) having a chip island (14i), flat conductors (horizontal portions of 14k) surrounding the chip island, and contact pillars (vertical portions of 14k) arranged on the flat conductors and aligned orthogonally with respect to the flat conductors; wherein the second semiconductor chip (16) is arranged with its second face (16B) on the chip island and wherein its contact pads

(16C) are electrically connected via bonding wire connections (20) to the flat conductors; wherein the first semiconductor chip (12) is surrounded by the contact pillars (vertical portions of 14K) and is arranged underneath the chip island (14i) such that pillar contact pads (14M) of the contact pillars, first face areas (face of 19 touching 10) of a plastic encapsulation compound (19) that embeds the semiconductor chips, the contact pillars and the flat conductor structure, and the active first face (can be connected in a flip-chip manner, col 4 ln 26-30) of the first semiconductor chip (12A), form an overall first face (10a), and wherein a wiring layer (10, 11A) is arranged on the overall upper face and electrically connects the semiconductor chips to one another via wiring lines (col 7 ln 14-15 and col 10 ln 8-10).

Hoffman does not specify that the first face area of the plastic encapsulation and the active first face of the first chip form an overall first face as described in the arguments and specification (the active face of the die and the surface of the encapsulant are planar), although Fig 6A does show a planar interface between items 19 and 10. Ma teaches formation of an encapsulation material for dice that is planar with the active surface of the die in order to increase surface area for trace formation (col 4 ln 1-5). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Ma on the device of Hoffman in order to increase surface area for trace formation.

5. With regards to claims **11-12 and 22-23**, Hoffman discloses in Fig 6A the component of claim 10, wherein the wiring layer (10) comprises a wiring level (11A) arranged on the overall first face (10A) and comprises outer contact pads (11B) that are

electrically connected via the wiring lines (11A) to the pillar contact pads (14M) of the contact pillars (vertical portions of 14K) and to the contact pads (12C) on the first semiconductor chip, and wherein solder balls (15) are arranged on the outer contact pads (11B).

6. With regards to claims **13-14 and 24-25**, Hoffman discloses in Fig 15 the component of claim 10 configured within a panel comprising a leadframe with additional electronic components arranged in rows and columns (col 12 ln 1-5) wherein the shape of the panel corresponds in its extent and extent markings to a standard semiconductor wafer (col 13 ln 8-15).

7. Regarding claim **15**, Hoffman discloses in Fig 15 a method for production of a panel for a plurality of electronic components comprising: producing leadframe with component positions arranged in rows and columns (col 12 ln 1-5), whereby a component position comprises a chip island and flat conductors which surround the chip island (see Fig 6A), as well as contact pillars, which are arranged on the flat conductors and are aligned orthogonally with respect to the flat conductors; applying a stacked semiconductor chip to the chip island of the component positions (steps 3-5 of Fig 15); producing bonding wire connections (step 6) between the flat conductors and contact pads on active first faces of the stacked semiconductor chips, with the first semiconductor chips being arranged in rows and columns which correspond to the rows and columns of the component positions; applying a wiring layer (10) to the overall upper face, forming wiring lines and outer contact pads; and wherein the wiring lines

connect the outer contact pads to the contact pads of the first semiconductor chip (see Fig 6A).

Hoffman does not specify applying first semiconductor chips with their active upper faces to a carrier with adhesive bonding on one side, applying the leadframe with stacked semiconductor chips to the carrier in such a way that the contact pillars of the leadframe are adhesively bonded by their first faces to the carrier and the first semiconductor chips are arranged on the carrier underneath the chip islands of the leadframe and are surrounded by contact pillars, embedding the leadframe with stacked semiconductor chips and bonding wire connections in a plastic compound to form a composite body on the carrier; and removing the carrier exposing an overall upper face composed of active upper faces of the first semiconductor chips, pillar contact pads of the contact pillars, and an upper face of the plastic compound. Ma teaches formation of an encapsulation material for dice that is planar with the active surface of the die in order to increase surface area for trace formation (col 4 ln 1-5). The die is adhesively bonded by its active face to a carrier, encapsulated, and the carrier removed – forming a planar face of die and encapsulant. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Ma in the method of Hoffman in order to increase surface area for trace formation.

8. Regarding claim **16**, Hoffman discloses the method of claim 15 further comprising applying solder balls to the outer contact pads to provide outer contacts (Fig 15 step 8).

9. Regarding claim **17**, Hoffman discloses the method of claim 15 further comprising separating the panel into individual electronic components (Fig 15 step 9).

10. Regarding claim **18**, Hoffman discloses the method of claim 17, further comprising applying outer contact pads of an electronic component (see Fig 6A item 11b).

***Response to Arguments***

11. Applicant's arguments filed 26 June 2007 have been fully considered but they are not persuasive.

Regarding the argument on page 6 that there does not appear to be any additional surface area for trace formation when comparing figures of the references, Hoffman discloses that the first die may be flip chip mounted (col 4 ln 26-30) and Ma further teaches that having encapsulation material for dice that is planar with the active surface of the die increases surface area for trace formation (col 4 ln 1-5).

Regarding the argument on page 8, Hoffman discloses that the first die (12) may be flip chip mounted (col 4 ln 26-30) in encapsulant (19), resulting in an active face (12a) of the first die being exposed on the outside of the encapsulant, and Ma teaches that having encapsulation material (112 is encapsulant, not a substrate) for dice that is planar with the active surface of the die (102) increases surface area for trace formation (col 4 ln 1-5). Therefore the operation of the Hoffman device is unchanged and the purpose of the encapsulant is the same (both encapsulate the body of a die and expose the active face).

Regarding the argument on page 9 that Hoffman requires the inactive side of the die be attached to the die pad, Hoffman discloses that the first die (12) may alternatively be electrically connected in a flip chip manner (col 4 ln 26-30). Regarding the argument on pages 9 and 10 that the two references relate to different types of electronic components with different technical problems, both references relate to electronic packages. Hoffman discloses the component and encapsulation, while Ma teaches that having encapsulation material for dice that is planar with the active surface of the die increases surface area for trace formation (col 4 ln 1-5). The teaching and applications of Ma are applicable to the lower flip-chip die of the Hoffman stacked arrangement even though Ma is directed towards a single chip package.

***Conclusion***

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John C. Ingham whose telephone number is (571) 272-8793. The examiner can normally be reached on M-F, 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

John C Ingham
Examiner, Art Unit 2814

/Wai-Sing Louie/
Primary Examiner, Art Unit 2814

/J. C. I./